3W Mono Filterless Class-D Audio Power Amplifier

BA16852

Data Sheet

Rev.1.1, 2007.08.28

Biforst Technology Inc.

3W Mono Filterless Class-D Audio Power Amplifier

BA16852

GENERAL DESCRIPTION

The BA16852 is a cost-effective mono class-d audio power amplifier that assembles in 1.45mm x 1.45mm wafer chip scale package (CSP). Only three external components offer space and cost saving for cellular phone or PDA application. The BA16852 provides 3W high performance output capacity at 4-Ω load. Other feature like 90% efficiency, -75dB PSRR, fully differential design reduces RF rectification, and allows independent gain while summing signals from various audio sources. BA16852 also integrates Anti-Pop, Output Short & Over-Heat Protection Circuitry to increase device reliability. The functionality makes this device ideal for cellular phone, PDA, and other applications that demand more battery life.

FEATURE

- Wide Operation Voltage From 2.5 To 5.5V
- Efficiency with 8-Ω Speaker
  - 89% at 1.3W
  - 80% at 0.25W
- Output Driver Capability, 1.3W With 8-Ω Load And THD+N < 1%
- Output Driver Capability, 2.3W With 4-Ω Load And THD+N < 1%
- Low 1μA Shutdown Current
- Low 5mA Typical Quiescent Current
- PSRR, -75dB, No Need For Voltage Regulator
- Internally Generated 250KHz Switching Frequency Without External Capacitor And Resistor
- External Gain Configuration Capability
- Fully Differential Design For Eliminates Two Input Coupling Capacitors And Reduces RF Rectification
- Filterless PWM Output Technology without LC Output Filter
- Integrated Anti-Pop Circuitry
- Integrated Output Short Protection Circuitry
- Integrated Over-Heat Protection Circuitry
- Package Type : MSOP 8Pin

APPLICATION

- Cellular Phones
- PDA and Smart Phones
- Portable Electronic Device
- Portable Computer

APPLICATION CIRCUIT

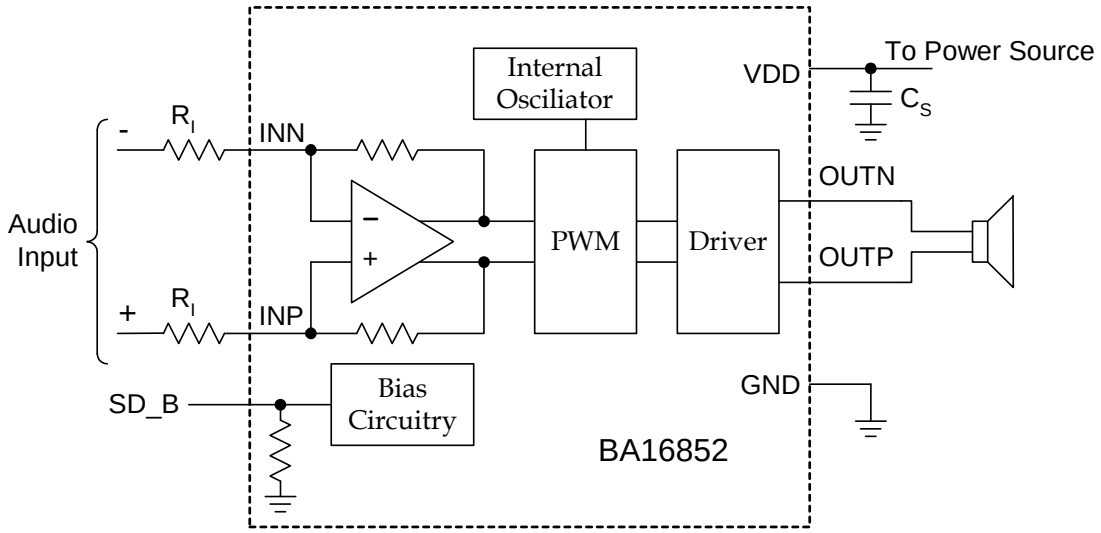
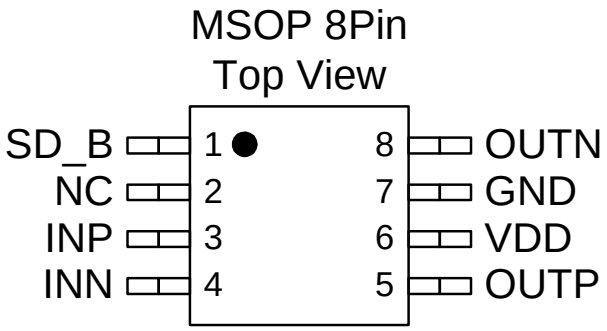


Figure 1. Typical BA16852 Application Circuit

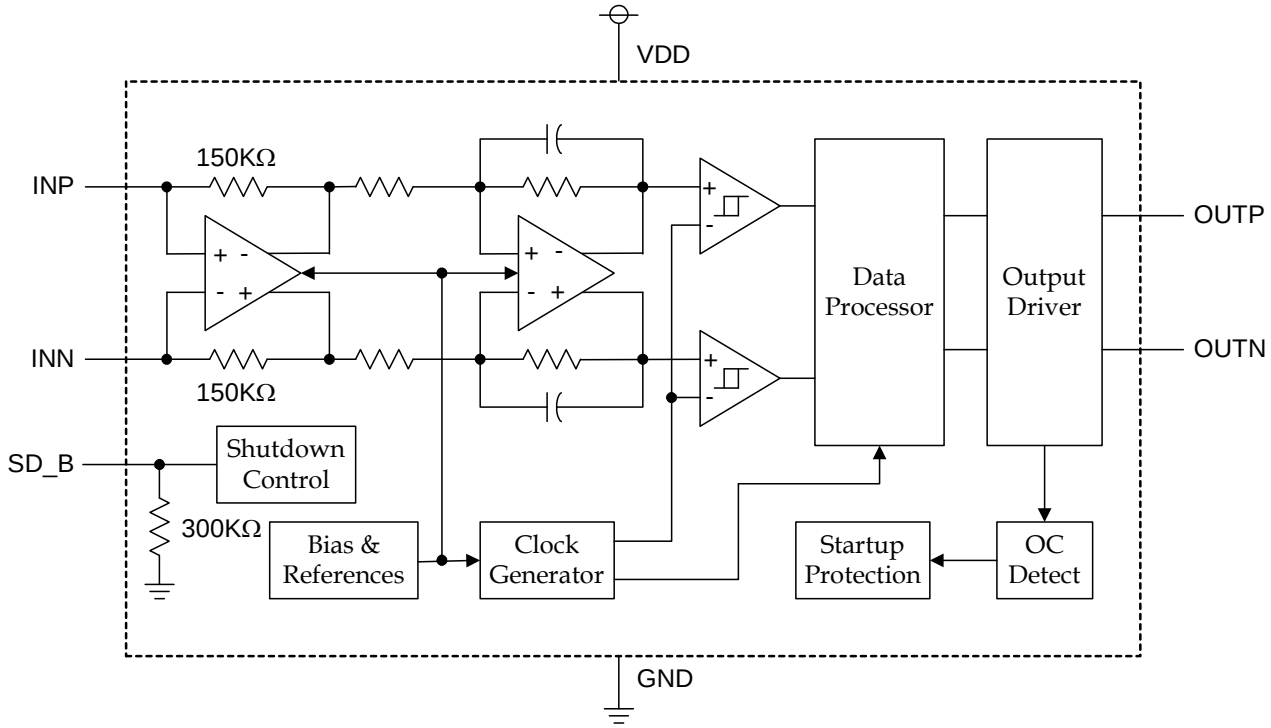
PIN ASSIGNMENT



PIN LIST & DESCRIPTION

Pin No.	Pin	Type	I/O Pad Function
1	SD_B	Input	Shutdown (Active Low Logic)
2	NC		
3	INP	Input	Positive differential audio input
4	INN	Input	Negative differential audio input
5	OUTP	Output	Positive BTL output
6	VDD	Power	Power supply
7	GND	Power	Power ground
8	OUTN	Output	Negative BTL output

Function Block Diagram



These device have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V_{DD}	Supply Voltage Range	-0.3V to 6V
V_I	Input Voltage Range	-0.3V to V_{DD}+0.3V
T_A	Operating Free-Air Temperature Range	-40°C to 85°C
T_J	Operating Junction Temperature Range	-40°C to 125°C
T_{STG}	Storage Temperature Range	-65°C to 150°C

RECOMMANDED OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{DD}	Supply Voltage		2.5	5.5	V
V_{IH}	High-Level Input Voltage	SHUTDOWN_B	2	V_{DD}	V
V_{IL}	Low-Level Input Voltage	SHUTDOWN_B	0	0.8	V
R_I	Input Resistor	GAIN ≤ 20V/V	15		kΩ
f_{PWM}	PWM Frequency		200	300	KHz
V_{IC}	Common Mode Input Voltage Range	VDD=2.5V, 5.5V, CMRR ≤ -49dB	0.5	V_{DD}-0.8	V
T_A	Operating Free-Air Temperature		-40	85	°C

ELECTRICAL CHARACTERISTICS

TA = 25°C (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output Offset Voltage (Measured Differentially)	V_I = 0V, A_V = 2V/V, V_{DD} = 2.5 to 5.5V			1	25	mV
PSRR	Power Supply Rejection Ratio	V_{DD} = 2.5 to 5.5V			-75	-55	dB
CMRR	Common Mode Rejection Ratio	V_{DD} = 2.5 to 5.5V, V_{IC} = 0.5V to V_{DD}-0.8V			-68	-49	
$\lvert I_{IH} \rvert$	High-Level Input Current	V_{DD} = 5.5V, V_I = 5.8V				100	μA
$\lvert I_{IL} \rvert$	Low-Level Input Current	V_{DD} = 5.5V, V_I = -0.3V				5	μA
$I_{(Q)}$	Quiescent Current	VDD = 5.5V, no load			5.8	6.2	mA
		VDD = 3.6V, no load			4.3	4.7	
		VDD = 2.5V, no load			3.1	3.4	
$I_{(SD)}$	Shutdown Current	$V_{(SHUTDOWN\_B)}$ = 0.35V, V_{DD} = 2.5 to 5.5V			0.5	2	μA
$r_{DS(ON)}$	Static Drain-Source On-State Resistance	V_{DD} = 5V, I_O = 500mA	High Side		450	650	mΩ
			Low Side				
$F_{(SW)}$	Switching Frequency	V_{DD} = 2.5 to 5.5V		200	250	300	kHz
	Gain	V_{DD} = 2.5 to 5.5V		$\frac{285k\Omega}{R_I}$	$\frac{300k\Omega}{R_I}$	$\frac{350k\Omega}{R_I}$	$\frac{V}{V}$
	Resistance from shutdown to GND				300		kΩ

OPWEATING CHARACTERISTICS

TA = 25°C , Gain = 2V/V, R_L = 3 / 4 / 8Ω (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output Power	THD+N = 10%, f = 1KHz, R_L = 3Ω	V_{DD} = 5V		3.6		W
			V_{DD} = 3.6V		1.8		
			V_{DD} = 2.5V		0.7		
		THD+N = 1%, f = 1KHz, R_L = 3Ω	V_{DD} = 5V		2.8		W
			V_{DD} = 3.6V		1.3		
			V_{DD} = 2.5V		0.56		
		THD+N = 10%, f = 1KHz, R_L = 4Ω	V_{DD} = 5V		3		
			V_{DD} = 3.6V		1.5		
			V_{DD} = 2.5V		0.66		
		THD+N = 1%, f = 1KHz, R_L = 4Ω	V_{DD} = 5V		2.3		
			V_{DD} = 3.6V		1.1		
			V_{DD} = 2.5V		0.48		
		THD+N = 10%, f = 1KHz, R_L = 8Ω	V_{DD} = 5V		1.7		W
			V_{DD} = 3.6V		0.89		
			V_{DD} = 2.5V		0.4		
		THD+N = 1%, f = 1KHz, R_L = 8Ω	V_{DD} = 5V		1.33		W
			V_{DD} = 3.6V		0.65		
			V_{DD} = 2.5V		0.3		
THD+N	Total Harmonic Distortion Plus Noise	V_{DD} = 5V, P_O = 1W, R_L = 8Ω, f = 1KHz			0.18%		
		V_{DD} = 3.6V, P_O = 0.5W, R_L = 8Ω, f = 1KHz			0.16%		
		V_{DD} = 3.0V, P_O = 0.2W, R_L = 8Ω, f = 1KHz			0.27%		
K_{SVR}	Supply Ripple Rejection Ration	V_{DD} = 3.6V, Input AC-Grounded with C_i = 2μF	f = 215Hz, $V_{(RIPPLE)}$ = 0.2V_{PP}		-67		dB
SNR	Signal-to-noise Ratio	V_{DD} = 5V, P_O = 1W, R_L = 8Ω			93		dB
V_n	Output Voltage Noise	V_{DD} = 3.6V, f = 20Hz to 20KHz, Input AC-Grounded with C_i = 2μF	No Weight		88		μV_{RMS}
			A Weight		63		
CMRR	Common Mode Rejection Ratio	V_{DD} = 3.6V, V_{IC} = 1V_{PP}	f = 217Hz		-63		dB
Z_I	Input Impedance			141	150	159	kΩ
	Start-up time from shutdown	V_{DD} = 3.6V			30		ms

TYPICAL CHARACTERISTIC

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	Supply Ripple Rejection Ratio vs. Frequency at 4Ω Load	25
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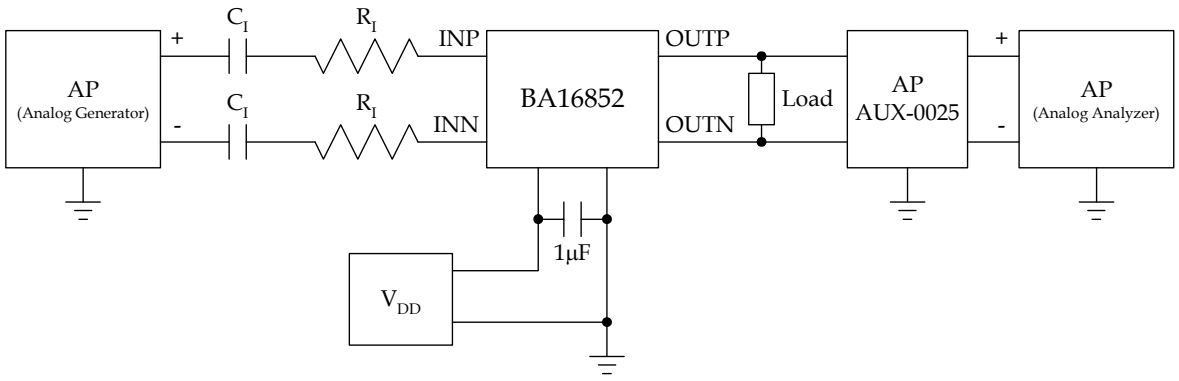
Test Set-Up For Graphs



Notes:

1. C_I was shorted for any Common-Mode input voltage measurement.
2. A 22μH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurement.
3. The AP AUX-0025 low-pass filter is required.
4. The 22-KHz or 30-KHz low-pass filter is required even if the AP analyzer has an internal low-pass filter.

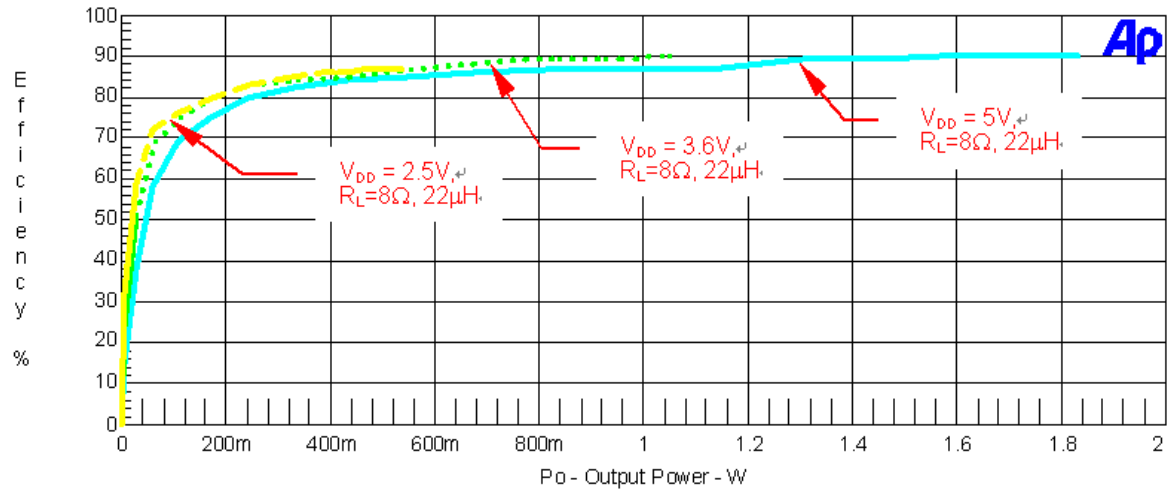


Figure 2. Efficiency vs. Output Power at 8Ω Load

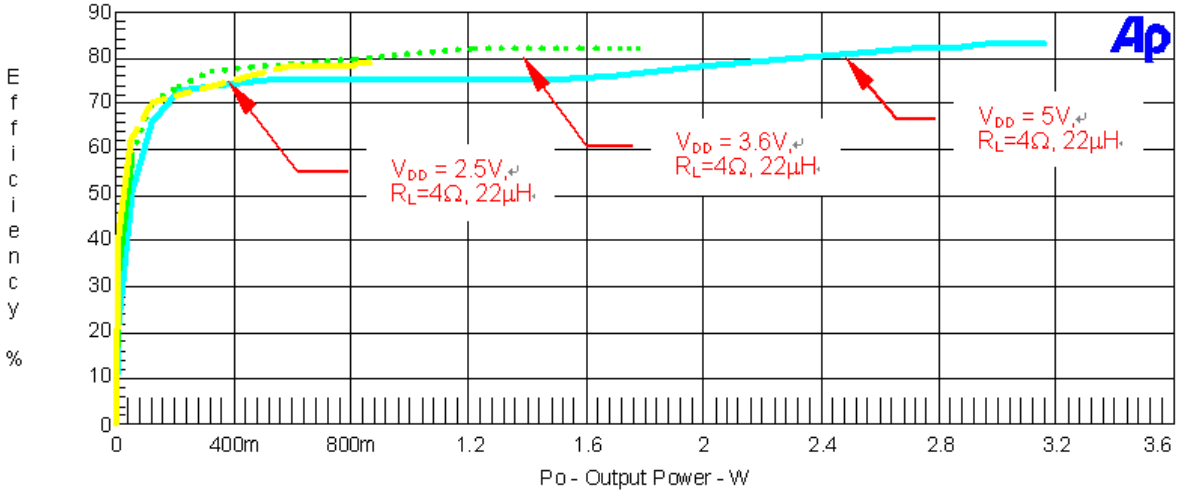


Figure 3. Efficiency vs. Output Power at 4Ω Load

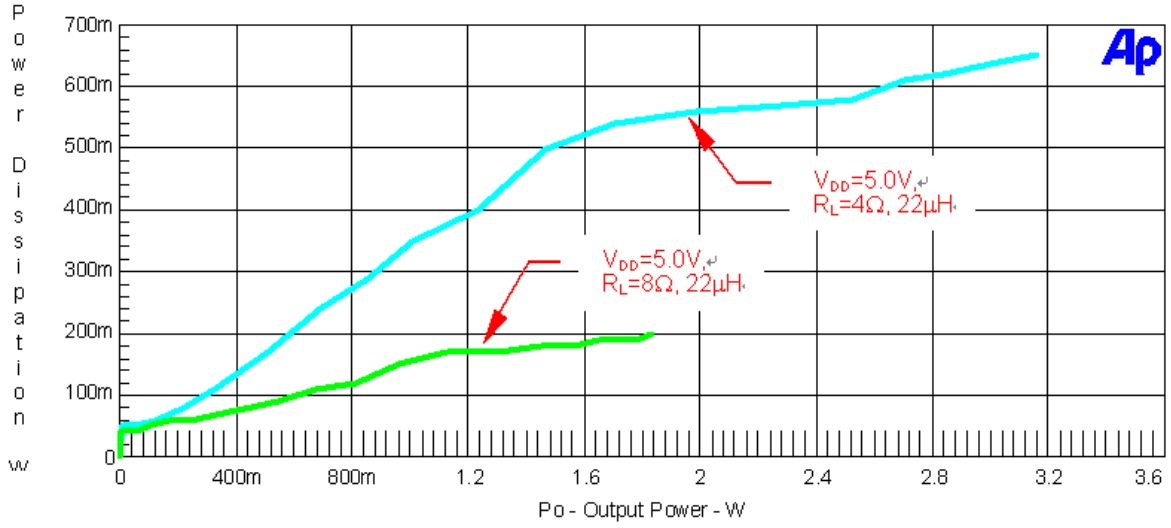


Figure 4. Power Dissipation vs. Output Power at 5.0V

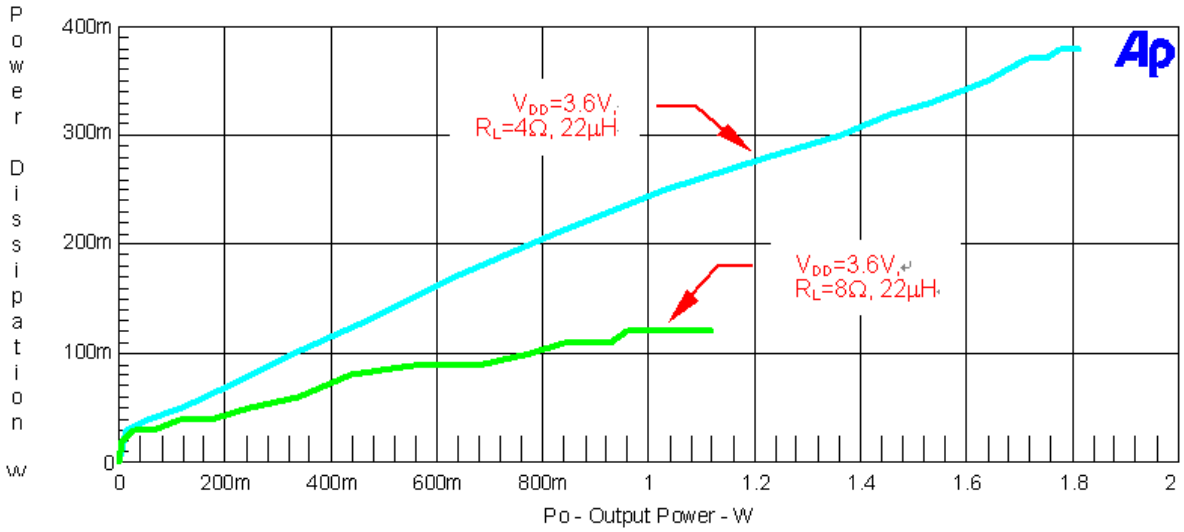


Figure 5. Power Dissipation vs. Output Power at 3.6V

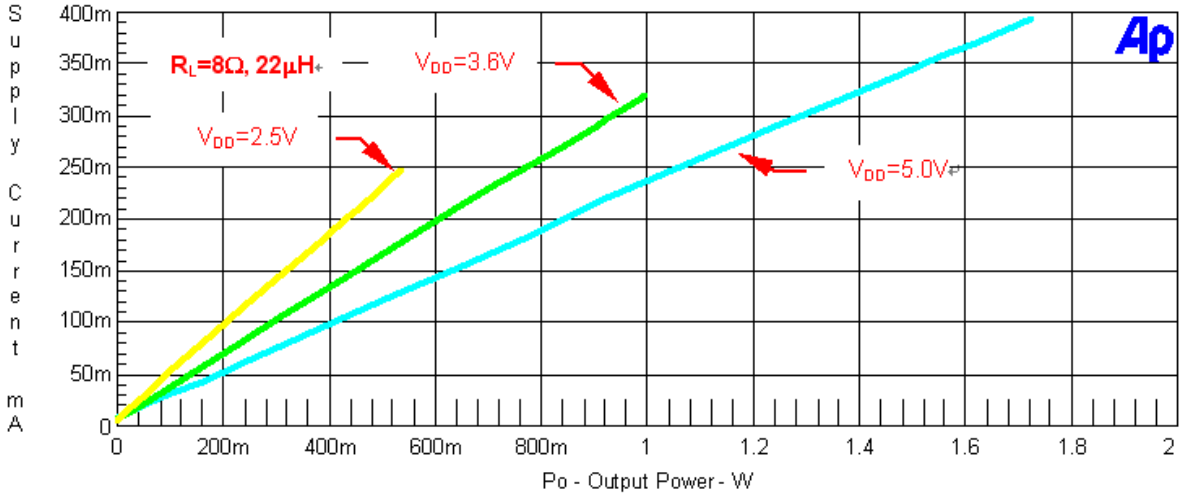


Figure 6. Supply Current vs. Output Power at 8Ω Load

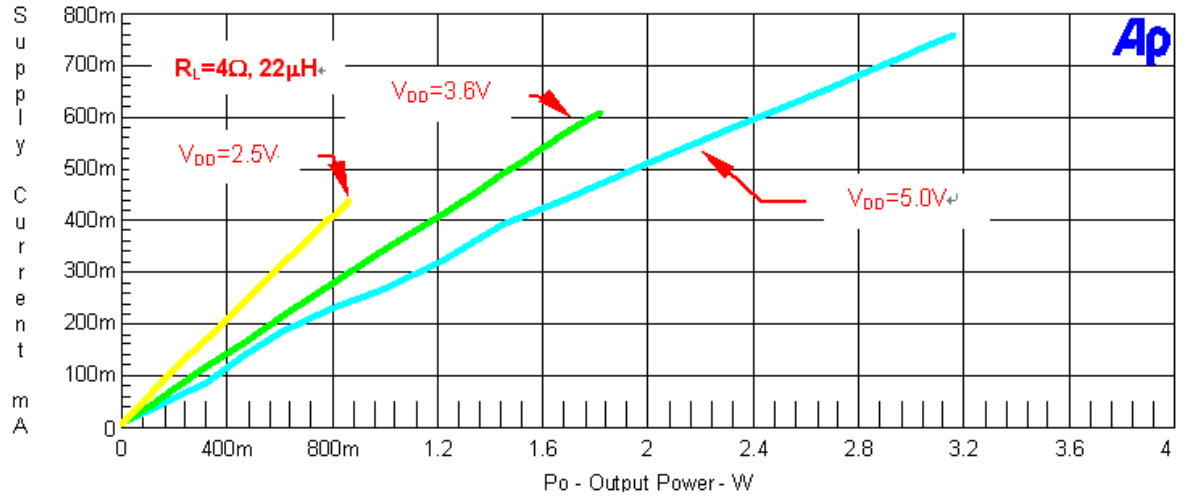


Figure 7. Supply Current vs. Output Power at 4Ω Load

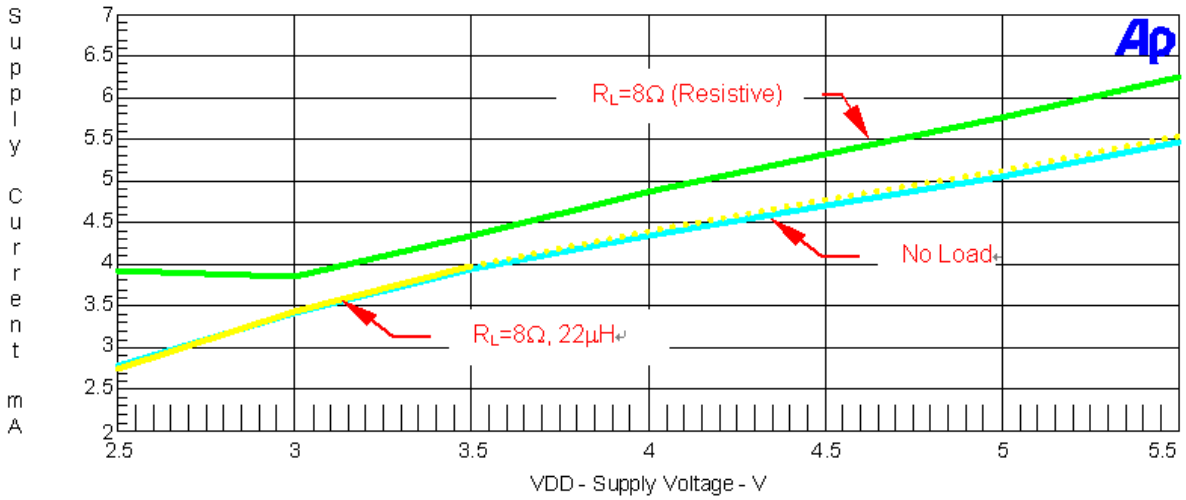


Figure 8. Quiescent Current vs. Supply Voltage

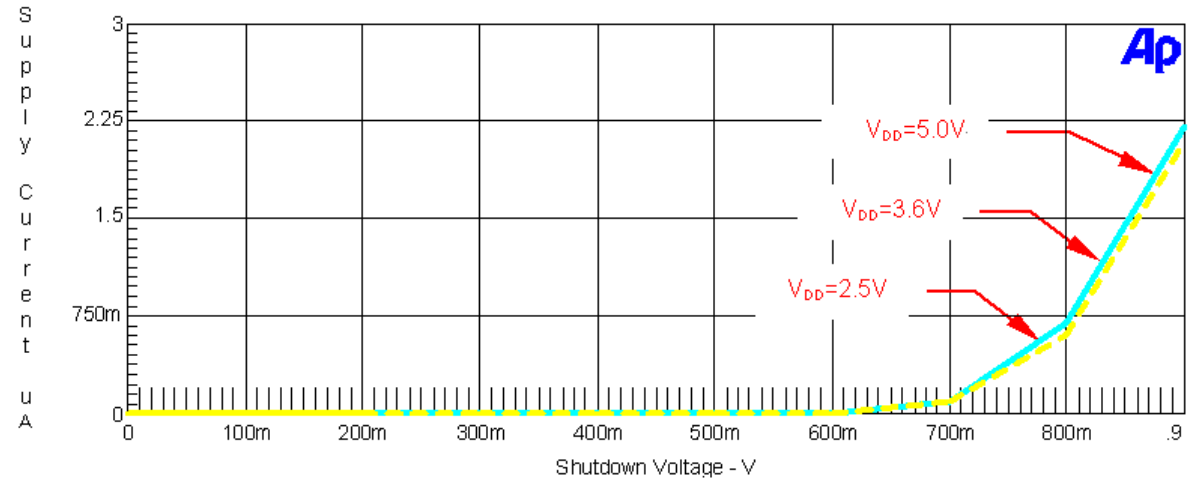


Figure 9. Shutdown Current vs. Shutdown Voltage

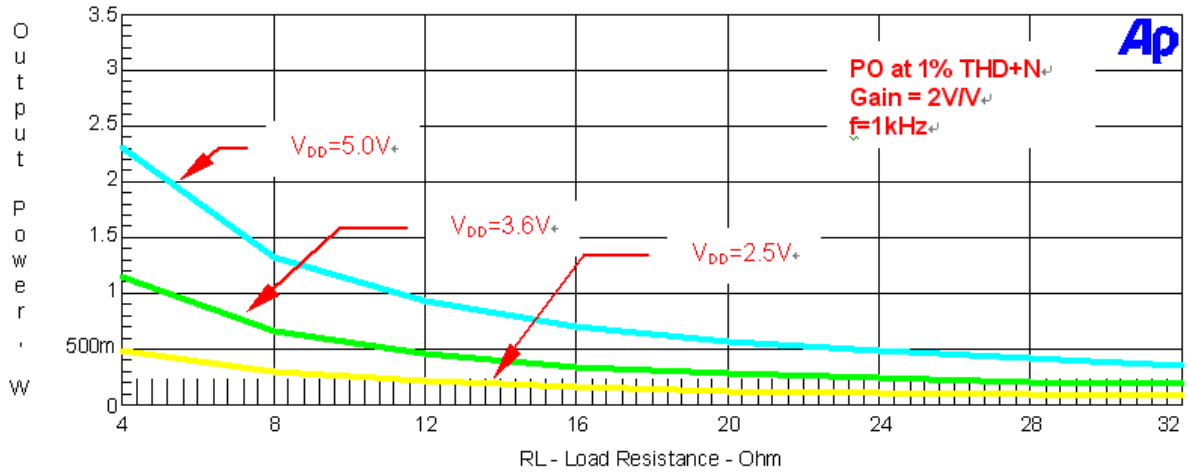


Figure 10. Output Power at 1% THD+N vs. Load Resistance

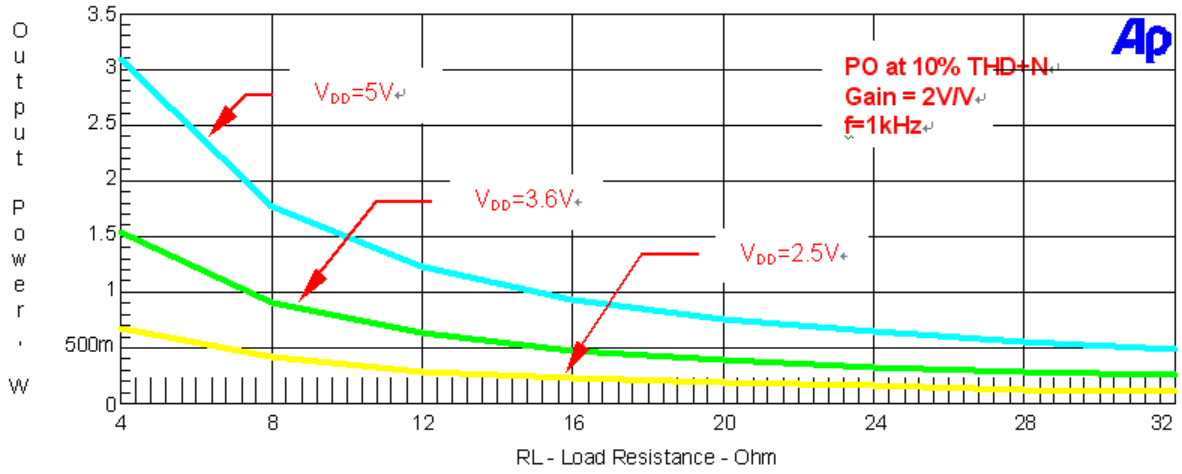


Figure 11. Output Power at 10% THD+N vs. Load Resistance

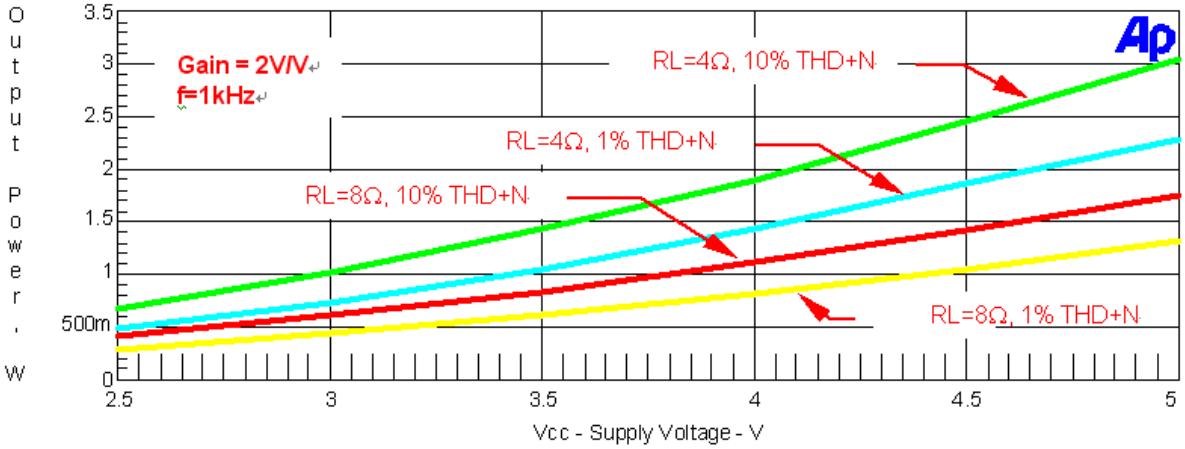


Figure 12. Output Power vs. Supply Voltage

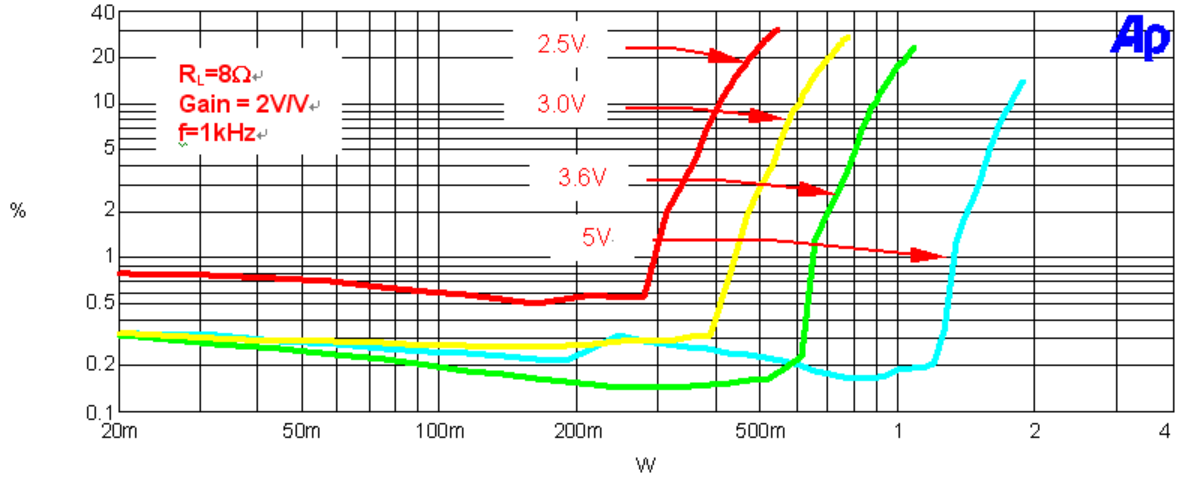


Figure 13. Total Harmonic Distortion + Noise vs. Supply Voltage at 8Ω Load

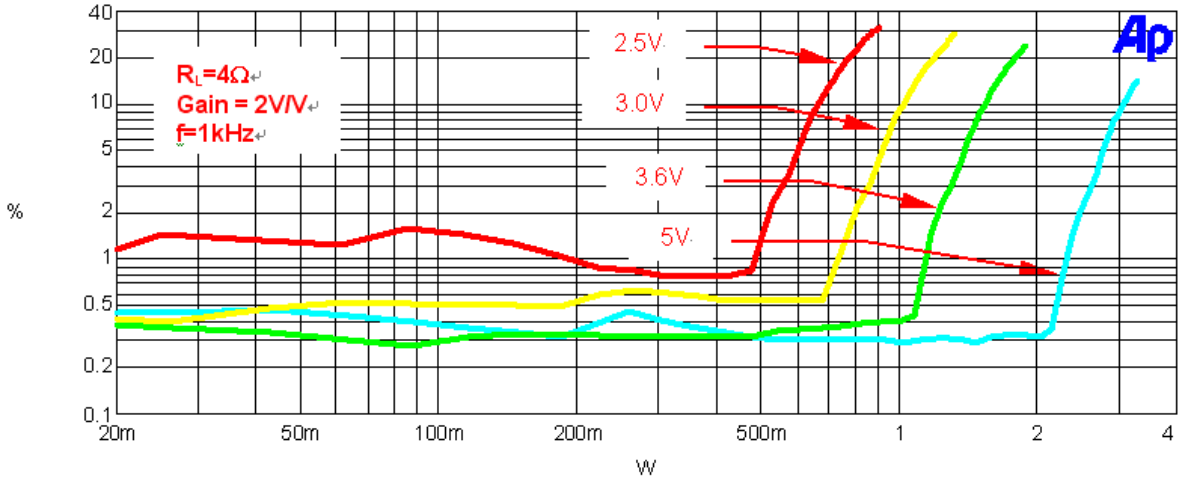


Figure 14. Total Harmonic Distortion + Noise vs. Supply Voltage at 4Ω Load

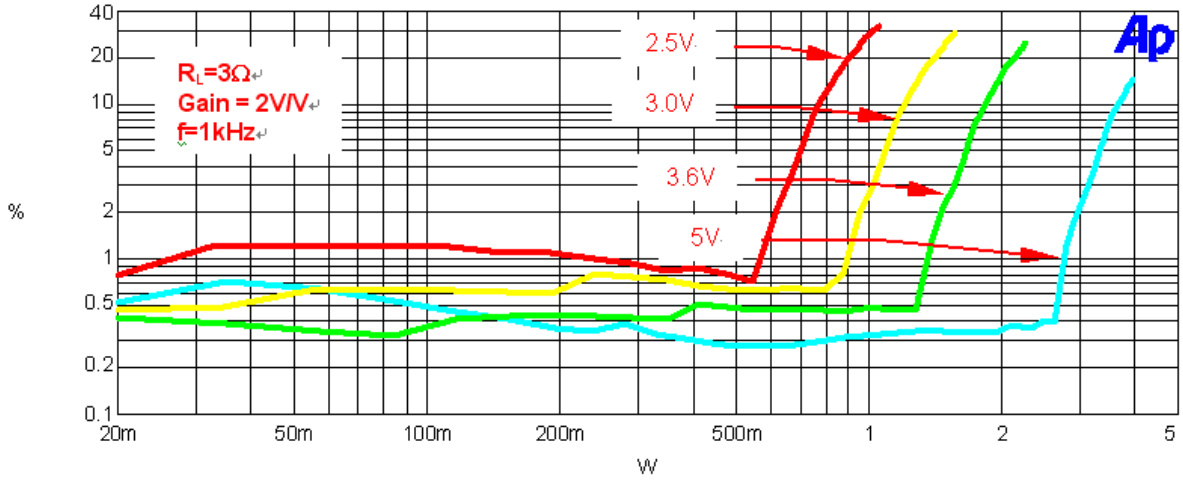


Figure 15. Total Harmonic Distortion + Noise vs. Supply Voltage at 3Ω Load

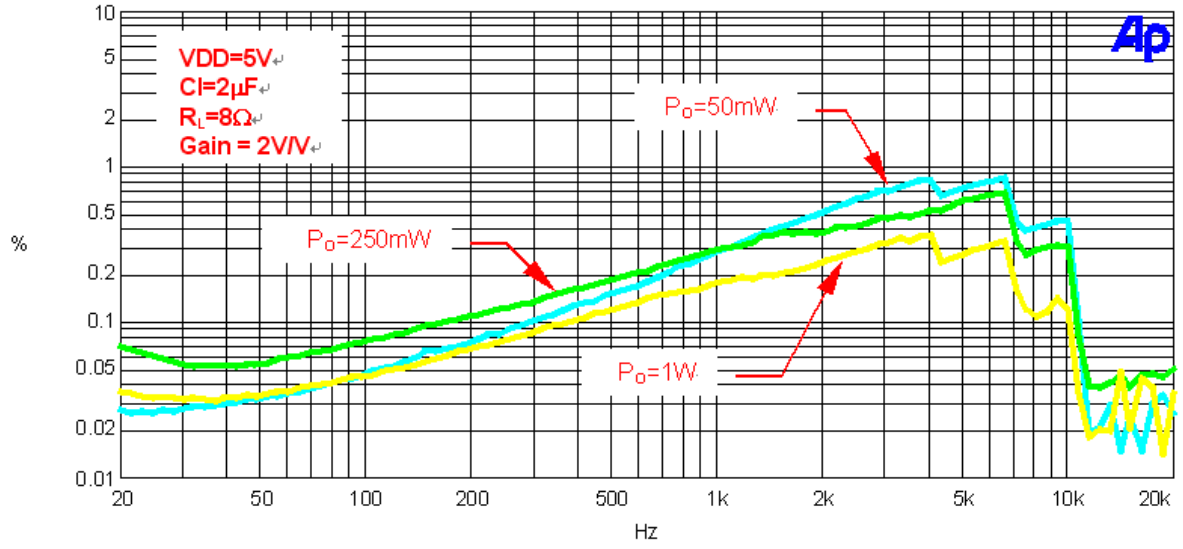


Figure 16. Total Harmonic Distortion + Noise vs. Frequency at 5.0V & 8Ω Load

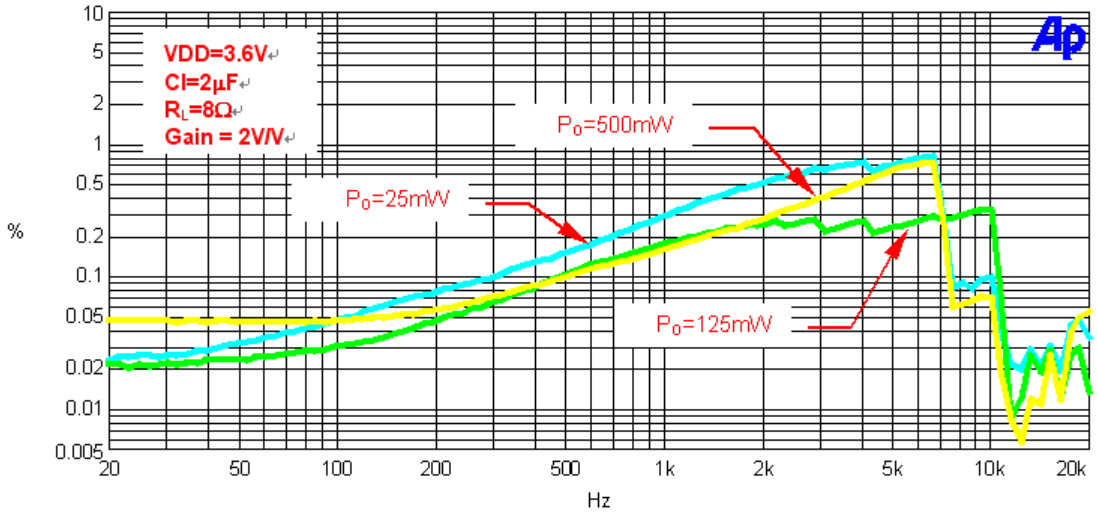


Figure 17. Total Harmonic Distortion + Noise vs. Frequency at 3.6V & 8Ω Load

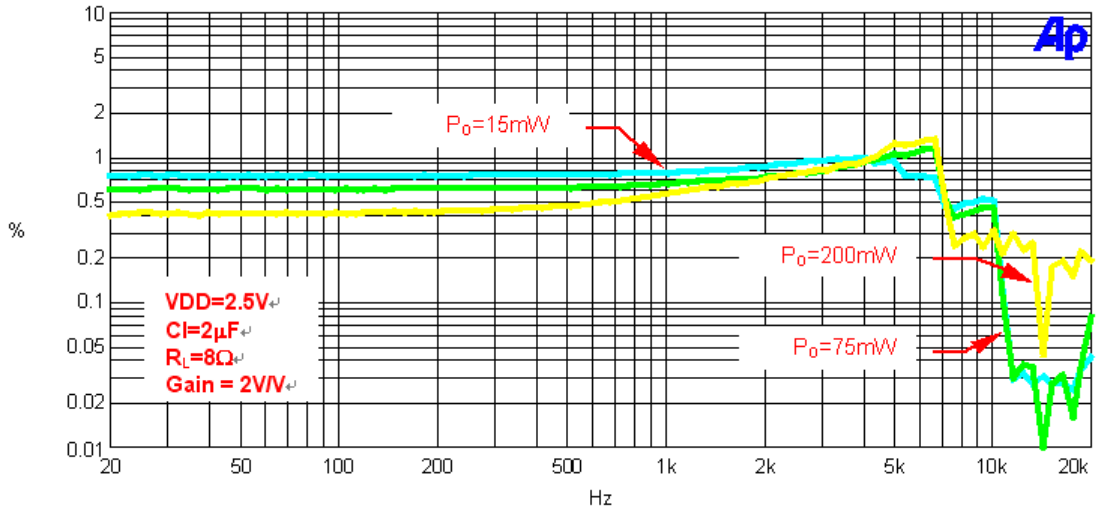


Figure 18. Total Harmonic Distortion + Noise vs. Frequency at 2.5V & 8Ω Load

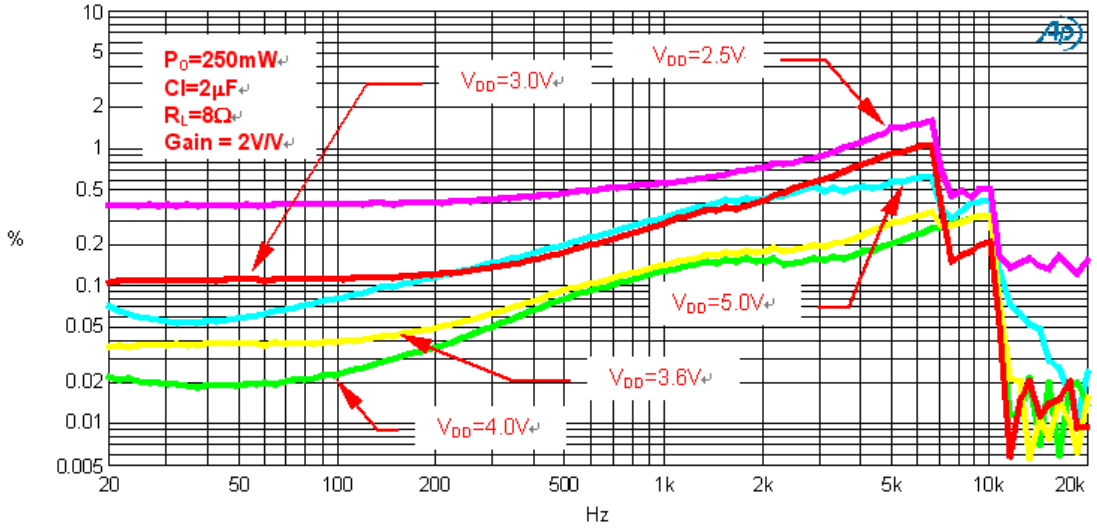


Figure 19. Total Harmonic Distortion + Noise vs. Frequency at 5/4/3.6/3/2.5V, 250mW Output, 8Ω Load

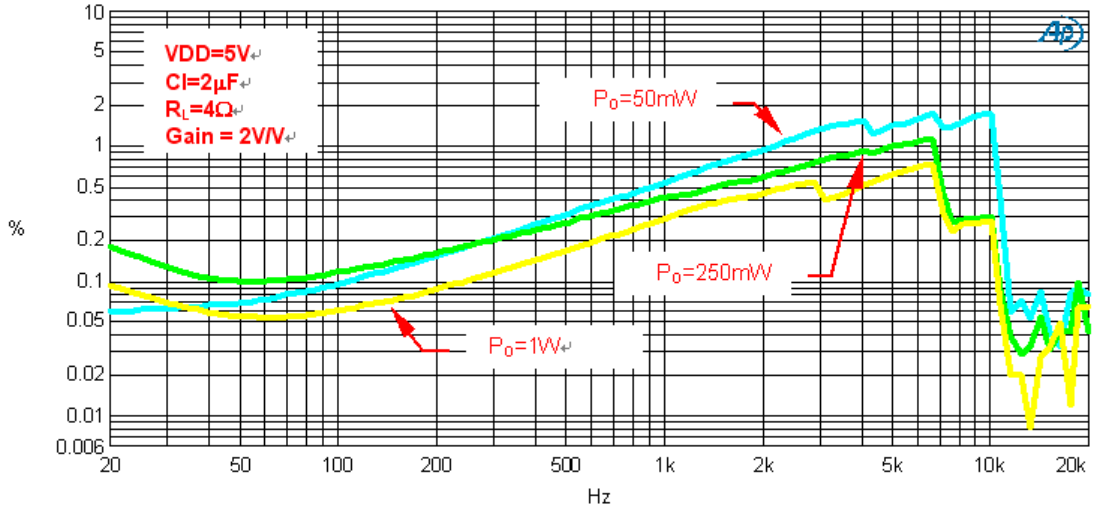


Figure 20. Total Harmonic Distortion + Noise vs. Frequency at 5.0V & 4Ω Load

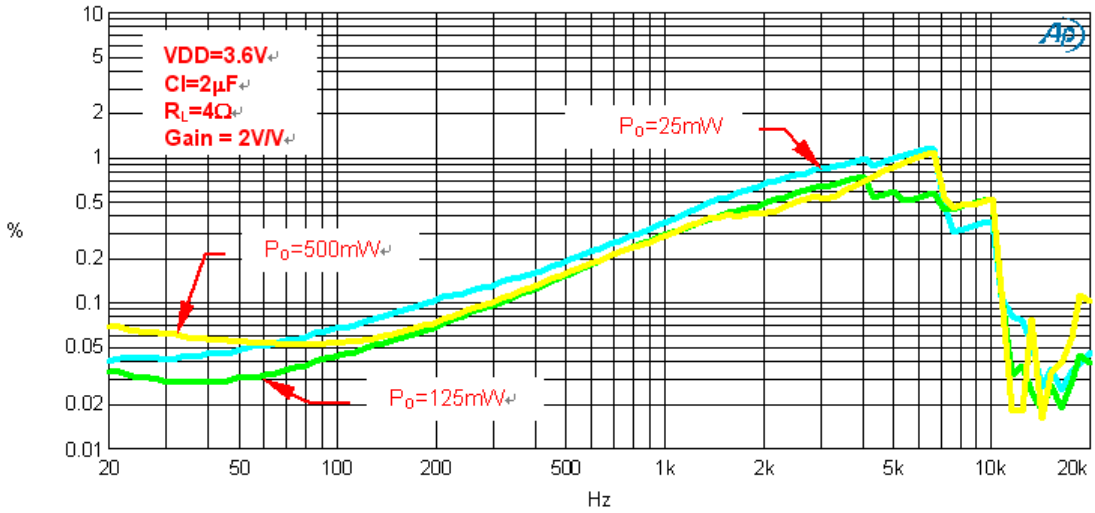


Figure 21. Total Harmonic Distortion + Noise vs. Frequency at 3.6V & 4Ω Load

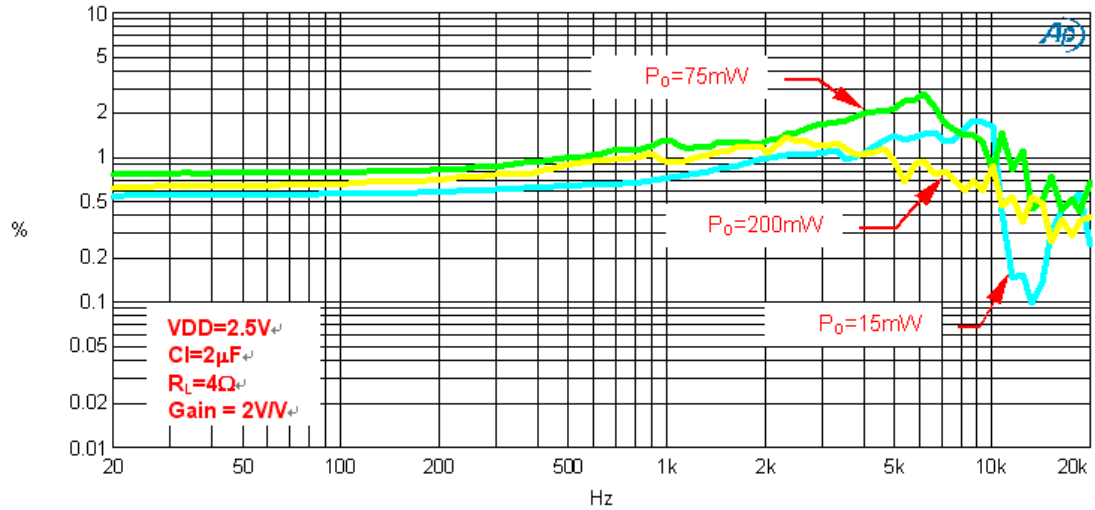


Figure 22. Total Harmonic Distortion + Noise vs. Frequency at 2.5V & 4Ω Load

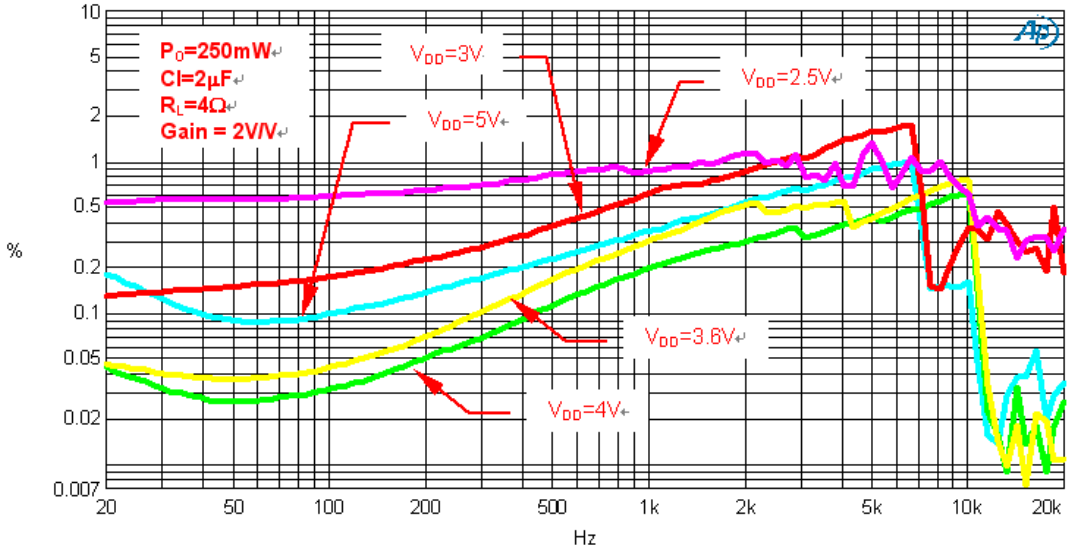


Figure 23. Total Harmonic Distortion + Noise vs. Frequency at 5/4/3.6/3/2.5V, 250mW Output, 4Ω Load

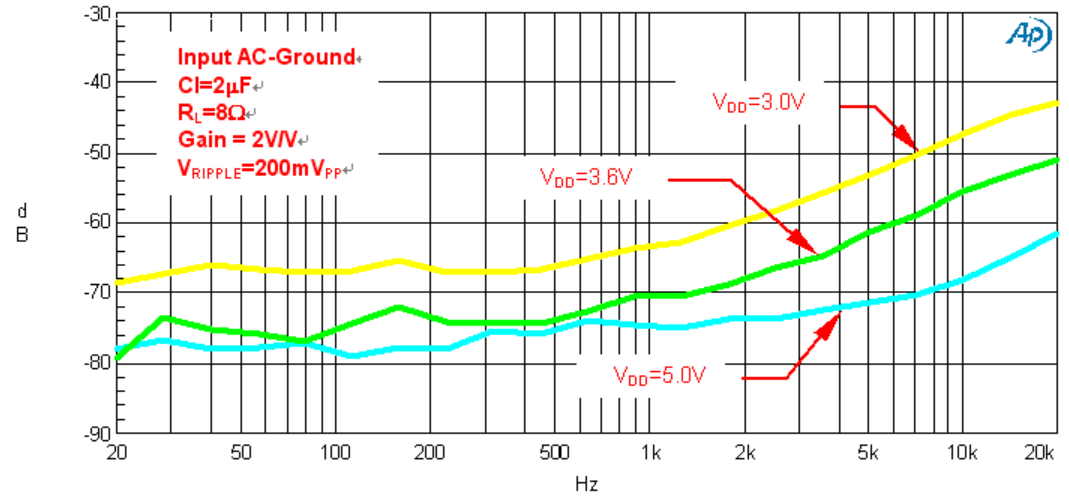


Figure 24. Supply Ripple Rejection Ration vs. Frequency at 8Ω Load

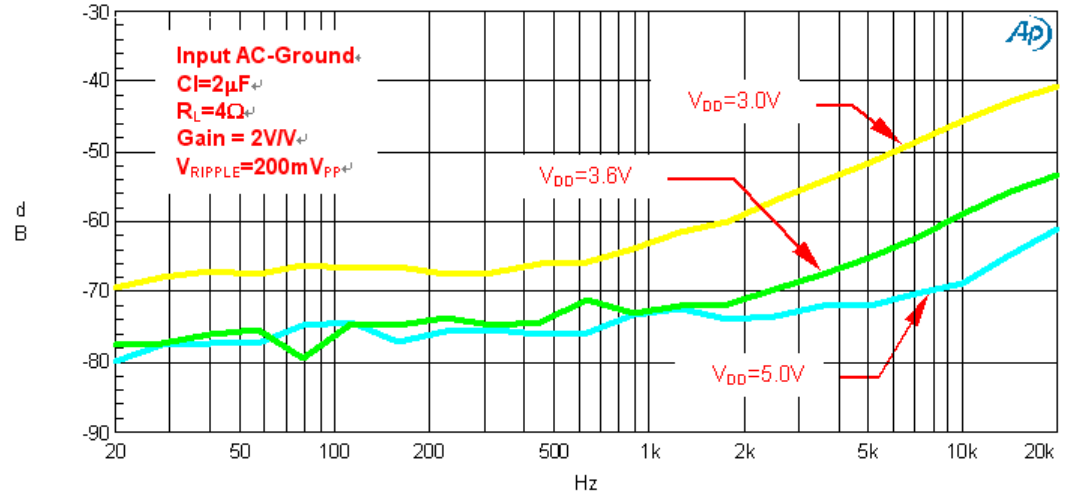


Figure 25. Supply Ripple Rejection Ration vs. Frequency at 4Ω Load

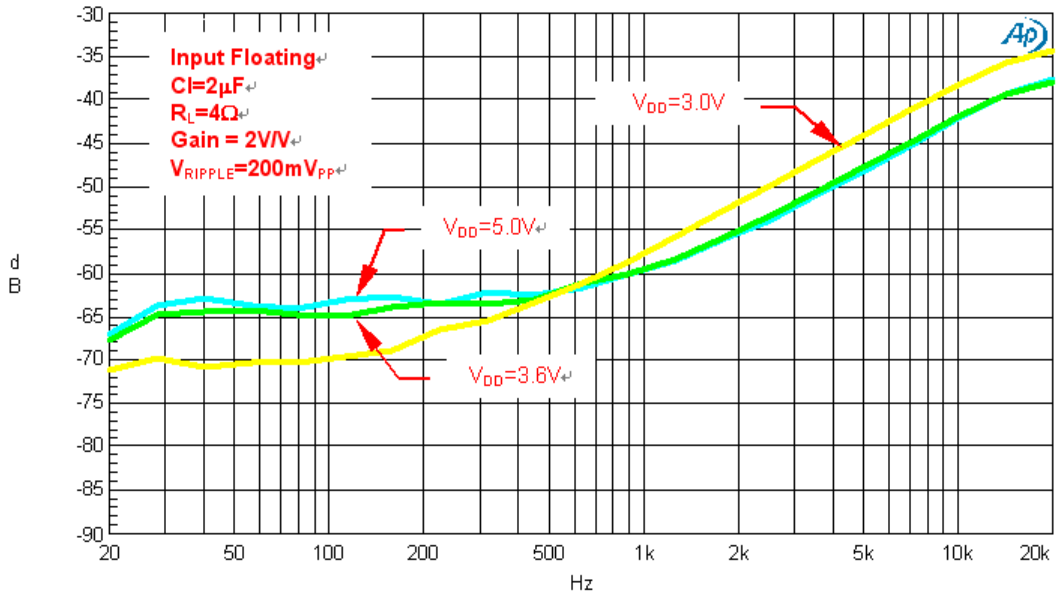


Figure 26. Supply Ripple Rejection Ration vs. Frequency at Input Floating

Function Description

The basic structure of BA16852 is a differential amplifier with differential inputs and outputs. The BA16852 has one differential amplifier and one common-mode amplifier inside. The differential amplifier output a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The BA16852 can still be used with a single ended input. The BA16852 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Input Resistors (R_I)

The gain of BA16852 is set by external resistors R_I show in Figure 1. Set the gain of the amplifier according to Equation (1)

$$\text{Gain} = \frac{2\times 150\text{k}\Omega}{R_I} \quad (\frac{V}{V}) \qquad (1)$$

The gain should be set to 2 V/V or lower for best performance. Lower gain allows the BA16852 use a high voltage at input and make the input less susceptible to noise.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. It is recommended to use 1% tolerance resistor or better for best performance. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

The R_I resistor should be placed close to the BA16852 and keep the input traces close to each other with the same length in high noise environment. It can limit noise injection on the high-impedance nodes.

Power Supply Decoupling Capacitor (C_S)

As with any power amplifier, proper power supply decoupling capacitor is critical for low noise performance and high power supply rejection ration (PSRR). A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the BA16852 is very important for the efficiency of the class-d amplifier, because any resistance or inductance in the trace between the device and capacitor can cause a loss in efficiency.

Input Capacitor (C_I)

The input capacitor may be needed for some applications or when the source is single-ended (See Figure 28). This capacitor can block the DC voltage at the amplifier input terminal and create a high-pass filter with the input resistor R_I. The cut-off frequency of high-pass filter is according to Equation (2)

$$f_C = \frac{1}{2\pi \times R_I \times C_I} \text{ (Hz)} \qquad (2)$$

The value of the input capacitor affects the low frequency performance of the circuit directly. Speakers in wireless phone can't respond well to low frequency, so the cut-off frequency can be set to block low frequency in this application. For example, power supply noise is at 217Hz in a GSM phone. Setting cut-off frequency of high-pass filter above 217Hz can filter out this noise that it is not amplified and heard on the output. Capacitor has 10% tolerance or better is recommended for impedance matching.

Differential Circuit Configurations

The BA16852 can be used in many different circuit configurations. The simplest and best performing is the DC coupled, differential input configuration show in Figure 27. The resistor R_I can set the amplifier output gain. Set the gain of the amplifier according to Equation (1).

The input capacitors can be used in a differential configure as show in Figure 28. The input capacitor C_I with input resistor R_I can create a high-pass filter. The cut-off frequency of high-pass filter is according to Equation (2). Equation (1) above is used to determine the value of the R_I resistors for a desired gain.

The BA16852 can be used to amplify more than one audio source. Figure 29 shows a dual differential input configuration. The gain for each input source can be set independently according to Equation (3) and (4).

$$\text{Gain } 1 = \frac{2\times 150\text{k}\Omega}{R_{I1}} \quad (\frac{V}{V}) \qquad (3)$$

$$\text{Gain } 2 = \frac{2\times 150\text{k}\Omega}{R_{I2}} \quad (\frac{V}{V}) \qquad (4)$$

The input capacitors can be used with one or more input source as well to have different frequency responses depending on the source or if a DC voltage needs to be blocked from the source.

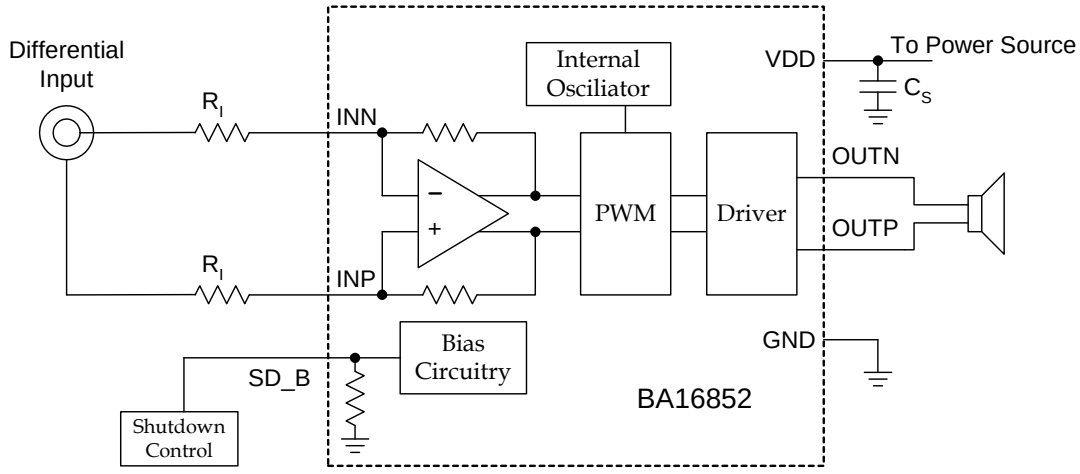


Figure 27. Differential Input Configuration

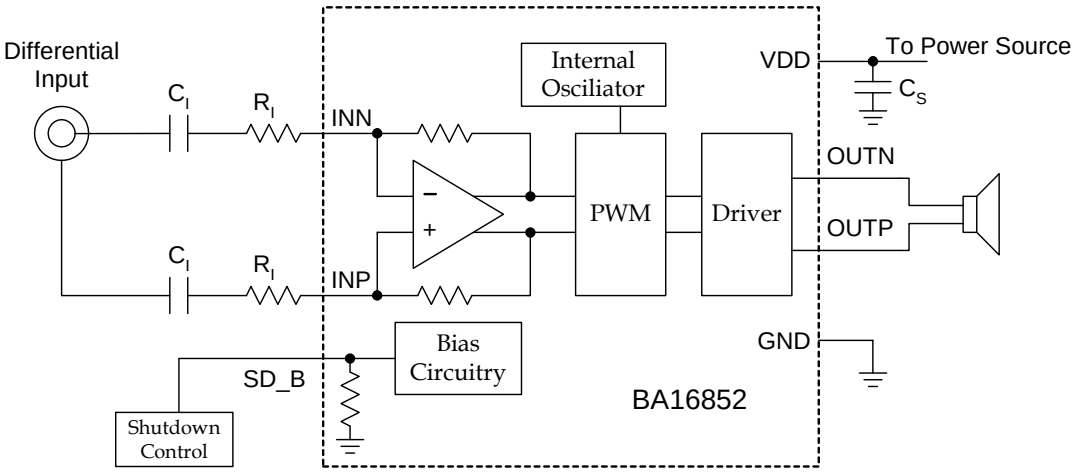


Figure 28. Differential Input Configuration with Input Capacitors

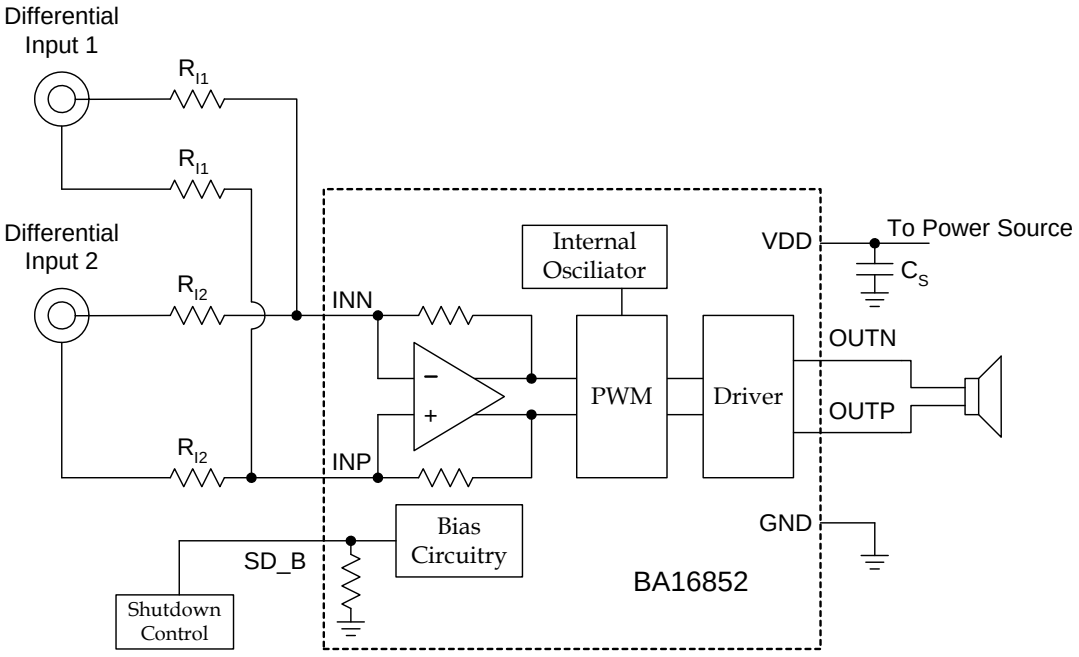


Figure 29. Dual Differential Input Configuration

Single-Ended Circuit Configurations

The BA16852 can also be used with single-ended sources, but input capacitors will be needed to block any DC at the input terminals. The typical single-ended application configuration shows in Figure 30. The equation of gain is Equation (1) and the equation of frequency response is Equation (2), hold for the single-ended configuration as shown in Figure 30.

When using more than one single-ended source as shown in Figure 31. The gain and cut-off frequency (f_{C1} and f_{C2}) for each input source can be set independently, shows in Equation (5) ~ Equation (8). Resistor, R_{I3}, and capacitor, C_{I3}, are needed on the INP terminal to match the impedance on the INN terminal. Equation (9) and Equation (10) shows how to calculate C_{I3} and R_{I3} value. The single-ended inputs must be driven by low impedance source even if one of the inputs is not outputting an ac signal.

$$\text{Gain 1} = \frac{2\times 150\text{k}\Omega}{R_{I1}} \quad (\frac{V}{V}) \qquad (5)$$

$$\text{Gain 2} = \frac{2\times 150\text{k}\Omega}{R_{I2}} \quad (\frac{V}{V}) \qquad (6)$$

$$f_{C1} = \frac{1}{2\pi \times R_{I1} \times C_{I1}} \quad (\text{Hz}) \qquad (7)$$

$$f_{C2} = \frac{1}{2\pi \times R_{I2} \times C_{I2}} \quad (\text{Hz}) \qquad (8)$$

$$C_{I3} = C_{I1} + C_{I2} \qquad (9)$$

$$R_{I3} = \frac{1}{(\frac{1}{R_{I1}} + \frac{1}{R_{I2}})} = \frac{R_{I1} \times R_{I2}}{R_{I1} + R_{I2}} \qquad (10)$$

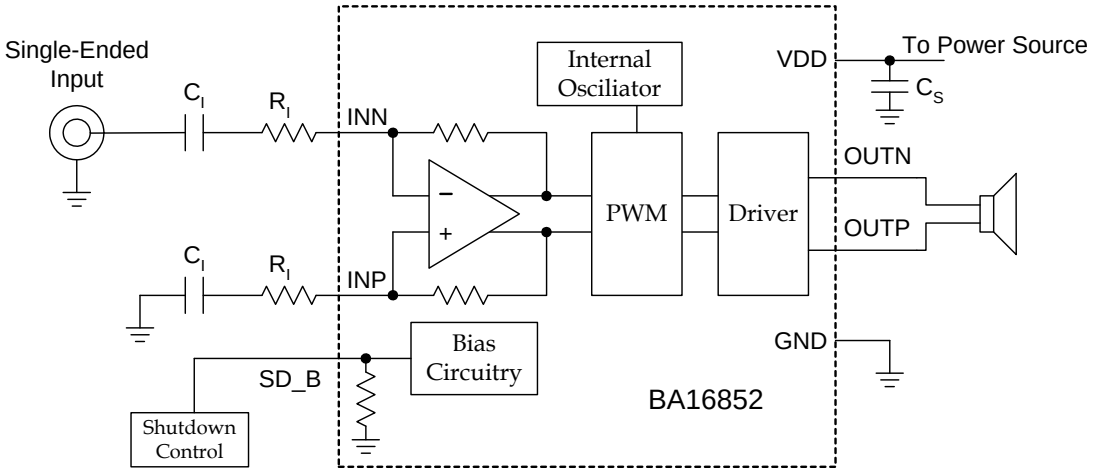


Figure 30. Single-Ended Input Configuration

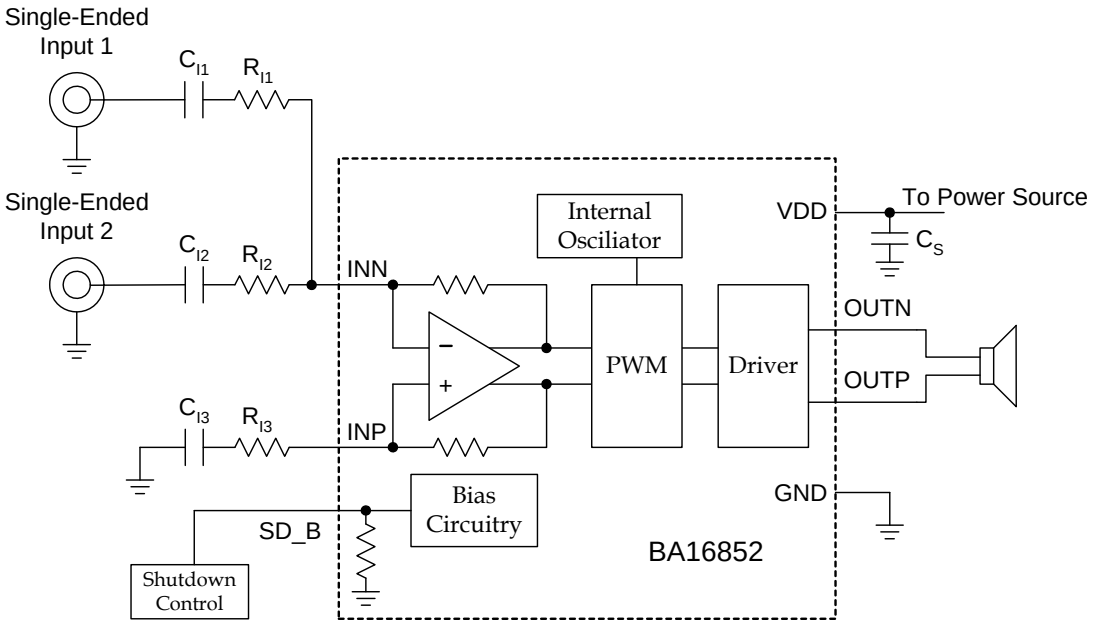


Figure 31. Dual Single-Ended Input Configuration

Combine Single-Ended & Differential Circuit Configurations

A typical application with one single-ended source and one differential source shows in Figure 32. Ground noise can couple in through INP terminal with this method. It is better to use dual differential inputs. The cut-off frequency of the single-ended input is set by C_I shows in Equation (13). To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$\text{Gain } 1 = \frac{2\times 150\text{k}\Omega}{R_{I1}} \quad (\frac{V}{V}) \qquad (11)$$

$$\text{Gain } 2 = \frac{2\times 150\text{k}\Omega}{R_{I2}} \quad (\frac{V}{V}) \qquad (12)$$

$$f_{C2} = \frac{1}{2\pi \times R_{I2} \times C_I} \quad \text{(Hz)} \qquad (13)$$

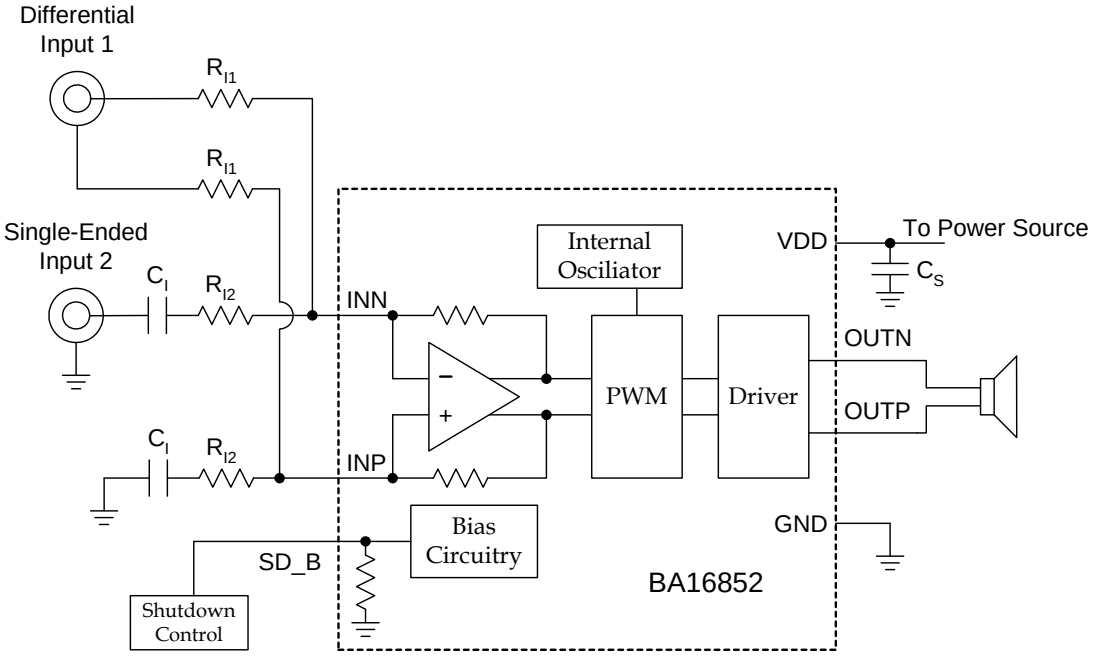


Figure 32. Dual Input with a Single-Ended Input and a Differential Input Configuration

Shutdown Mode

The BA16852 provides a shutdown mode for reduce supply current to the absolute minimum level during periods of nonuse for battery-power conservation. The BA16852 has an internal 300kΩ resistor connected between GND and SD_B pins. The purpose of this resistor is to eliminate any unwanted state changes when shutdown pin is floating. The SD_B input pin should be held high during normal operation when the amplifier is in use. Pulling SD_B low or left floating causes the outputs to mute and the amplifier to enter a low-current state. During the shutdown mode, the DC quiescent current of the circuit does not exceed 0.5μA.

Output Filter Application Note

Design the BA16852 without the filter if the traces from amplifier to speaker are short (<100mm). Where the speaker is in the same enclosure as the amplifier is a typical application for class-d without a filter. Like wireless handsets and PDAs are great applications for class-d without a filter.

Many applications require a ferrite bead filter. The ferrite filter reduces EMI around 30 MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and there are long wires from the amplifier to the speaker.

Figure 33 & 34 show typical LC and ferrite bead output filters.

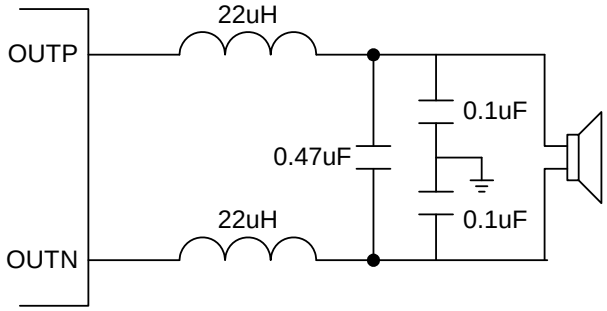


Figure 33. Typical LC Output Filter

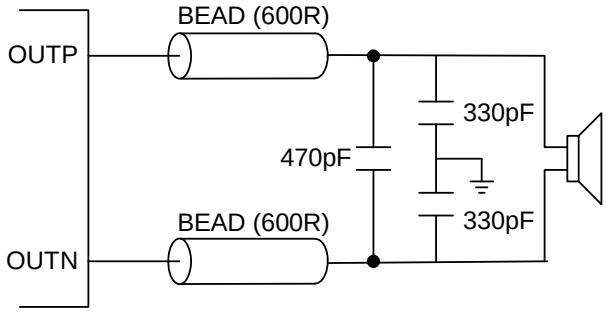


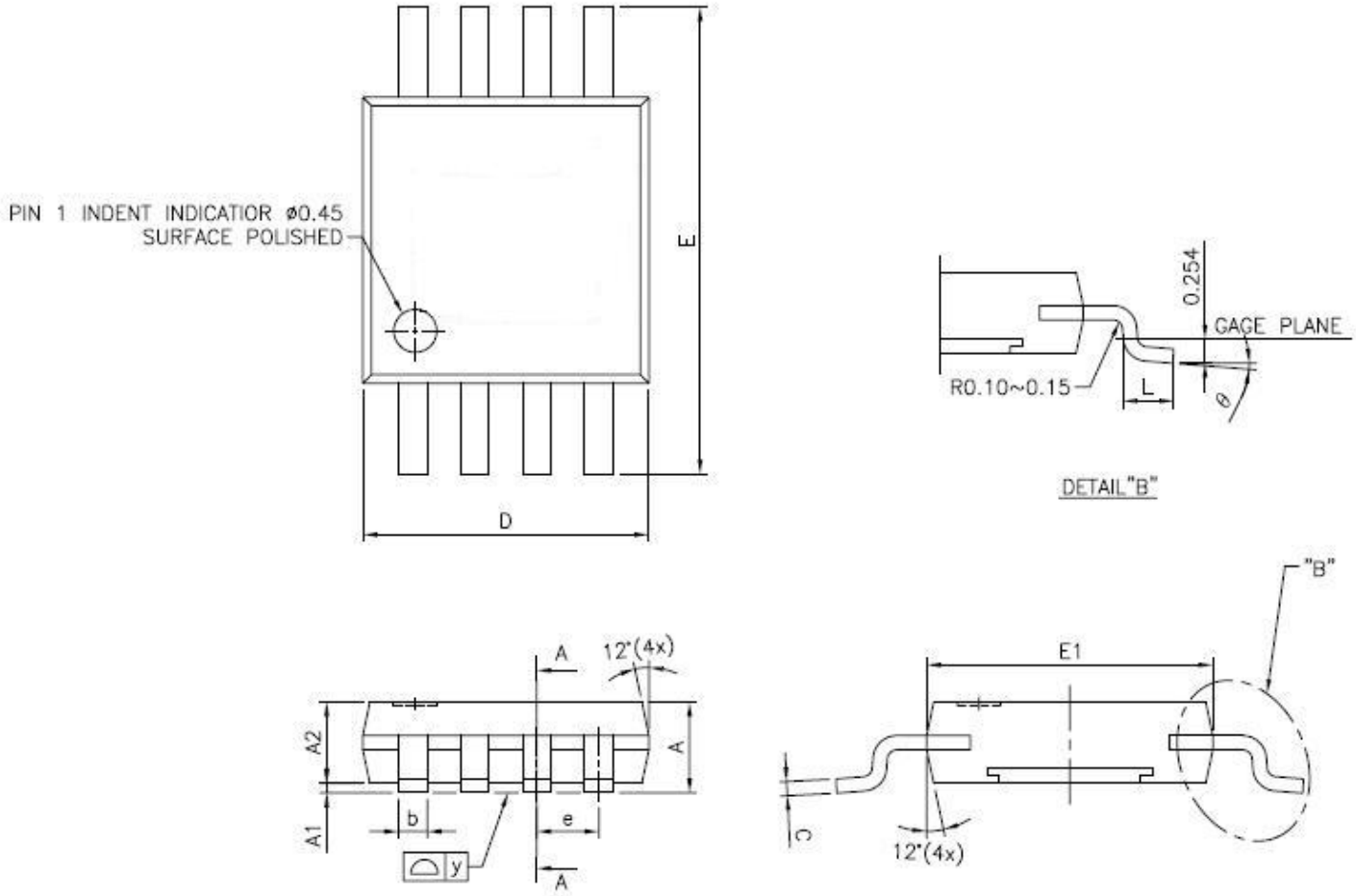
Figure 34. Typical Ferrite Chip Bead Output Filter
(Chip bead example : Queen Core / TI321611U601)

Board Layout Considerations

Place all the external components very close to the BA16852. Placing the decoupling capacitor, C_S, close to the BA16852 V_{DD} terminal is very important for the efficiency of the class-d amplifier. Any resistance and inductance in the trace between the device and the capacitor can cause a loss in efficiency. Additionally, the input resistors need to be very close to the BA16852 input terminal, so noise does not couple on the high-impedance nodes between the input resistors and the input amplifier of the BA16852.

PACKAGE DIMENSION

8PIN MSOP PACKAGE



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.05	—	0.15	0.002	—	0.006
A2	0.76	0.85	0.95	0.030	0.033	0.037
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	—	0.65	—	—	0.0256	—
L	0.40	0.53	0.66	0.016	0.021	0.026
y	—	—	0.10	—	—	0.004
θ	0°	3°	6°	0°	3°	6°

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